

CPLD 2 Specification

64 port G-PON

ASGvOLT64

(GPON OLT)

Version: 1.0

Revision History

Document Rev.	Date	Author	Revision Description	CPLD code version
1.0	8/29/2019		Initial OCP release	

3.1. Offset 0x01 CPLD version (Read Only)

Example : version 5.01 then reg 0x2 is 5, reg 0x3 is 1

Bit	Name	R/W	Reset Value	Description
7:0	CPLD_ver[7:0]	R	1	CPLD version

3.2. Offset 0x02 CPLD version (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	CPLD_ver[7:0]	R	0	CPLD version

3.3. Offset 0x03 SFP_ABS_1 (Read Only)

Bit	Front port	Name	R/W	Reset Value	Description
7	PON Port 22	MPL2_SFP29_MOD_ABS	R	1	0: SFP transceiver is present 1: SFP transceiver is absent
6	PON Port 23	MPL2_SFP28_MOD_ABS	R	1	0: SFP transceiver is present 1: SFP transceiver is absent
5	PON Port 26	MPL2_SFP27_MOD_ABS	R	1	0: SFP transceiver is present 1: SFP transceiver is absent
4	PON Port 27	MPL2_SFP26_MOD_ABS	R	1	0: SFP transceiver is present 1: SFP transceiver is absent
3	PON Port 30	MPL2_SFP25_MOD_ABS	R	1	0: SFP transceiver is present 1: SFP transceiver is absent
2	PON Port 31	MPL2_SFP24_MOD_ABS	R	1	0: SFP transceiver is present 1: SFP transceiver is absent
1	PON Port 29	MPL2_SFP23_MOD_ABS	R	1	0: SFP transceiver is present 1: SFP transceiver is absent
0	PON Port 28	MPL2_SFP22_MOD_ABS	R	1	0: SFP transceiver is present 1: SFP transceiver is absent

3.4. Offset 0x04 SFP_ABS_1 Mask (Read& Write)

(TBD)

Bit	Front port	Name	R/W	Reset Value	Description
7	PON Port 22	MASK*MPL2_SF P29_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
6	PON Port 23	MASK*MPL2_SF P28_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
5	PON Port 26	MASK*MPL2_SF P27_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
4	PON Port 27	MASK*MPL2_SF P26_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
3	PON Port 30	MASK*MPL2_SF P25_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
2	PON Port 31	MASK*MPL2_SF P24_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
1	PON Port 29	MASK*MPL2_SF P23_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
0	PON Port 28	MASK*MPL2_SF P22_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU

3.5. Offset 0x05 SFP_ABS_2 (Read Only)

Bit	Front port	Name	R/W	Reset Value	Description
7	PON Port 41	MPL3_SFP37_MOD_ABS	R	1	0: SFP transceiver is present 1: SFP transceiver is absent
6	PON Port 40	MPL3_SFP36_MOD_ABS	R	1	0: SFP transceiver is present 1: SFP transceiver is absent
5	PON Port 37	MPL3_SFP35_MOD_ABS	R	1	0: SFP transceiver is present 1: SFP transceiver is absent

4	PON Port 36	MPL3_SFP34_MOD_ABS	R	1	0: SFP transceiver is present 1: SFP transceiver is absent
3	PON Port 33	MPL3_SFP33_MOD_ABS	R	1	0: SFP transceiver is present 1: SFP transceiver is absent
2	PON Port 32	MPL3_SFP32_MOD_ABS	R	1	0: SFP transceiver is present 1: SFP transceiver is absent
1	PON Port 18	MPL2_SFP31_MOD_ABS	R	1	0: SFP transceiver is present 1: SFP transceiver is absent
0	PON Port 19	MPL2_SFP30_MOD_ABS	R	1	0: SFP transceiver is present 1: SFP transceiver is absent

3.6. Offset 0x06 SFP_ABS_2 Mask (Read& Write)

(TBD)

Bit	Front port	Name	R/W	Reset Value	Description
7	PON Port 41	MASK*MPL3_SF P37_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
6	PON Port 40	MASK*MPL3_SF P36_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
5	PON Port 37	MASK*MPL3_SF P35_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
4	PON Port 36	MASK*MPL3_SF P34_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
3	PON Port 33	MASK*MPL3_SF P33_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
2	PON Port 32	MASK*MPL3_SF P32_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
1	PON Port 18	MASK*MPL2_SF P31_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
0	PON Port 19	MASK*MPL2_SF P30_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU

3.7. Offset 0x07 SFP_ABS_3 (Read Only)

Bit	Front port	Name	R/W	Reset Value	Description
7:5		Reserved			
4	PON Port 43	MPL3_SFP42_MOD_ABS	R	1	0: SFP transceiver is present 1: SFP transceiver is absent
3	PON Port 46	MPL3_SFP41_MOD_ABS	R	1	0: SFP transceiver is present 1: SFP transceiver is absent
2	PON Port 47	MPL3_SFP40_MOD_ABS	R	1	0: SFP transceiver is present 1: SFP transceiver is absent
1	PON Port 45	MPL3_SFP39_MOD_ABS	R	1	0: SFP transceiver is present 1: SFP transceiver is absent
0	PON Port 44	MPL3_SFP38_MOD_ABS	R	1	0: SFP transceiver is present 1: SFP transceiver is absent

3.8. Offset 0x08 SFP_ABS_3 Mask (Read& Write)

(TBD)

Bit	Front port	Name	R/W	Reset Value	Description
7:5		Reserved			
4	PON Port 43	MASK*MPL3_SF P42_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
3	PON Port 46	MASK*MPL3_SF P41_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
2	PON Port 47	MASK*MPL3_SF P40_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
1	PON Port 45	MASK*MPL3_SF P39_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
0	PON Port 44	MASK*MPL3_SF P38_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU

3.9. Offset 0x09 SFP28_ABS (Read Only)

Bit	Front port	Name	R/W	Reset Value	Description
7	25G Port 7	SFP28_P7_MOD_ABS	R	1	0: SFP28 transceiver is present 1: SFP28 transceiver is absent
6	25G Port 6	SFP28_P6_MOD_ABS	R	1	0: SFP28 transceiver is present 1: SFP28 transceiver is absent
5	25G Port 5	SFP28_P5_MOD_ABS	R	1	0: SFP28 transceiver is present 1: SFP28 transceiver is absent
4	25G Port 4	SFP28_P4_MOD_ABS	R	1	0: SFP28 transceiver is present 1: SFP28 transceiver is absent
3	25G Port 3	SFP28_P3_MOD_ABS	R	1	0: SFP28 transceiver is present 1: SFP28 transceiver is absent
2	25G Port 2	SFP28_P2_MOD_ABS	R	1	0: SFP28 transceiver is present 1: SFP28 transceiver is absent
1	25G Port 1	SFP28_P1_MOD_ABS	R	1	0: SFP28 transceiver is present 1: SFP28 transceiver is absent
0	25G Port 0	SFP28_P0_MOD_ABS	R	1	0: SFP28 transceiver is present 1: SFP28 transceiver is absent

3.10. Offset 0x10 SFP28_ABS Mask (Read& Write)

(TBD)

Bit	Front port	Name	R/W	Reset Value	Description
7	25G Port 7	MASK*SFP28_P7_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
6	25G Port 6	MASK*SFP28_P6_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
5	25G Port 5	MASK*SFP28_P5_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU

4	25G Port 4	MASK*SFP28_P4 _MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
3	25G Port 3	MASK*SFP28_P3 _MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
2	25G Port 2	MASK*SFP28_P2 _MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
1	25G Port 1	MASK*SFP28_P1 _MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
0	25G Port 0	MASK*SFP28_P0 _MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU

3.11. Offset 0x11 SFP_TX_Fault_1 (Read only)

Bit	Front port	Name	R/W	Reset Value	Description
7	PON Port 22	MPL2_SFP29_TX_FAULT	R	1	1: SFP Transmit Fault 0: SFP Transmitter is working well
6	PON Port 23	MPL2_SFP28_TX_FAULT	R	1	1: SFP Transmit Fault 0: SFP Transmitter is working well
5	PON Port 26	MPL2_SFP27_TX_FAULT	R	1	1: SFP Transmit Fault 0: SFP Transmitter is working well
4	PON Port 27	MPL2_SFP26_TX_FAULT	R	1	1: SFP Transmit Fault 0: SFP Transmitter is working well
3	PON Port 30	MPL2_SFP25_TX_FAULT	R	1	1: SFP Transmit Fault 0: SFP Transmitter is working well
2	PON Port 31	MPL2_SFP24_TX_FAULT	R	1	1: SFP Transmit Fault 0: SFP Transmitter is working well
1	PON Port 29	MPL2_SFP23_TX_FAULT	R	1	1: SFP Transmit Fault 0: SFP Transmitter is working well
0	PON Port 28	MPL2_SFP22_TX_FAULT	R	1	1: SFP Transmit Fault 0: SFP Transmitter is working well

3.12. Offset 0x12 SFP_TX_Fault_1 Mask (Read& Write)

(TBD)

Bit	Front port	Name	R/W	Reset Value	Description
7	PON Port 22	MASK*MPL2_SFP27_TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault
6	PON Port 23	MASK*MPL2_SFP26_TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault
5	PON Port 26	MASK*MPL2_SFP25_TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault
4	PON Port 27	MASK*MPL2_SFP24_TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault
3	PON Port 30	MASK*MPL2_SFP23_TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault
2	PON Port 31	MASK*MPL2_SFP22_TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault
1	PON Port 29	MASK*MPL2_SFP27_TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault
0	PON Port 28	MASK*MPL2_SFP26_TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault

3.13. Offset 0x13 SFP_TX_Fault_2 (Read only)

Bit	Front port	Name	R/W	Reset Value	Description
7	PON Port 41	MPL3_SFP37_TX_FAULT	R	1	1: SFP Transmit Fault 0: SFP Transmitter is working well
6	PON Port 40	MPL3_SFP36_TX_FAULT	R	1	1: SFP Transmit Fault 0: SFP Transmitter is working well
5	PON Port 37	MPL3_SFP35_TX_FAULT	R	1	1: SFP Transmit Fault 0: SFP Transmitter is working well
4	PON Port 36	MPL3_SFP34_TX_FAULT	R	1	1: SFP Transmit Fault 0: SFP Transmitter is working well
3	PON	MPL3_SFP33_TX_FAULT	R	1	1: SFP Transmit Fault

	Port 33				0: SFP Transmitter is working well
2	PON Port 32	MPL3_SFP32_TX_FAULT	R	1	1: SFP Transmit Fault 0: SFP Transmitter is working well
1	PON Port 18	MPL2_SFP31_TX_FAULT	R	1	1: SFP Transmit Fault 0: SFP Transmitter is working well
0	PON Port 19	MPL2_SFP30_TX_FAULT	R	1	1: SFP Transmit Fault 0: SFP Transmitter is working well

3.14. Offset 0x14 SFP_TX_Fault_2 Mask (Read& Write)

(TBD)

Bit	Front port	Name	R/W	Reset Value	Description
7	PON Port 41	MASK*MPL3_SFP37_TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault
6	PON Port 40	MASK*MPL3_SFP36_TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault
5	PON Port 37	MASK*MPL3_SFP35_TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault
4	PON Port 36	MASK*MPL3_SFP34_TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault
3	PON Port 33	MASK*MPL3_SFP33_TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault
2	PON Port 32	MASK*MPL3_SFP32_TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault
1	PON Port 18	MASK*MPL2_SFP31_TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault
0	PON Port 19	MASK*MPL2_SFP30_TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault

3.15. Offset 0x15 SFP_TX_Fault_3 (Read only)

Bit	Front port	Name	R/W	Reset Value	Description
7:5		Reserved			

4	PON Port 43	MPL3_SFP42_TX_FAULT	R	1	1: SFP Transmit Fault 0: SFP Transmitter is working well
3	PON Port 46	MPL3_SFP41_TX_FAULT	R	1	1: SFP Transmit Fault 0: SFP Transmitter is working well
2	PON Port 47	MPL3_SFP40_TX_FAULT	R	1	1: SFP Transmit Fault 0: SFP Transmitter is working well
1	PON Port 45	MPL3_SFP39_TX_FAULT	R	1	1: SFP Transmit Fault 0: SFP Transmitter is working well
0	PON Port 44	MPL3_SFP38_TX_FAULT	R	1	1: SFP Transmit Fault 0: SFP Transmitter is working well

3.16. Offset 0x16 SFP_TX_Fault_3 Mask (Read& Write)

(TBD)

Bit	Front port	Name	R/W	Reset Value	Description
7:5		Reserved			
4	PON Port 43	MASK*MPL3_SFP42_TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault
3	PON Port 46	MASK*MPL3_SFP41_TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault
2	PON Port 47	MASK*MPL3_SFP40_TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault
1	PON Port 45	MASK*MPL3_SFP39_TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault
0	PON Port 44	MASK*MPL3_SFP38_TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault

3.17. Offset 0x17 SFP28_TX_Fault (Read only)

Bit	Front port	Name	R/W	Reset Value	Description
7	25G Port 7	SFP28_P7_TX_FAULT	R	1	1: SFP28 Transmit Fault 0: SFP28 Transmitter is working well
6	25G	SFP28_P6_TX_FAULT	R	1	1: SFP28 Transmit Fault

	Port 6				0: SFP28 Transmitter is working well
5	25G Port 5	SFP28_P5_TX_FAULT	R	1	1: SFP28 Transmit Fault 0: SFP28 Transmitter is working well
4	25G Port 4	SFP28_P4_TX_FAULT	R	1	1: SFP28 Transmit Fault 0: SFP28 Transmitter is working well
3	25G Port 3	SFP28_P3_TX_FAULT	R	1	1: SFP28 Transmit Fault 0: SFP28 Transmitter is working well
2	25G Port 2	SFP28_P2_TX_FAULT	R	1	1: SFP28 Transmit Fault 0: SFP28 Transmitter is working well
1	25G Port 1	SFP28_P1_TX_FAULT	R	1	1: SFP28 Transmit Fault 0: SFP28 Transmitter is working well
0	25G Port 0	SFP28_P0_TX_FAULT	R	1	1: SFP28 Transmit Fault 0: SFP28 Transmitter is working well

3.18. Offset 0x18 SFP28_TX_Fault Mask (Read& Write)

(TBD)

Bit	Front port	Name	R/W	Reset Value	Description
7	25G Port 7	MASK*SFP28_P7_TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault
6	25G Port 6	MASK*SFP28_P6_TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault
5	25G Port 5	MASK*SFP28_P5_TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault
4	25G Port 4	MASK*SFP28_P4_TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault
3	25G Port 3	MASK*SFP28_P3_TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault
2	25G Port 2	MASK*SFP28_P2_TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault
1	25G Port 1	MASK*SFP28_P1_TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault
0	25G	MASK*SFP28_P0_TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU

	Port 0	TX_FAULT			0: CPLD blocks incoming the Transmit Fault
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3.19. Offset 0x19 SFP_TX_Disable_1 (Read& Write)

Bit	Front port	Net Name	R/W	Reset Value	Description
7	PON Port 22	MPL2_SFP29_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off
6	PON Port 23	MPL2_SFP28_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off
5	PON Port 26	MPL2_SFP27_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off
4	PON Port 27	MPL2_SFP26_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off
3	PON Port 30	MPL2_SFP25_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off
2	PON Port 31	MPL2_SFP24_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off
1	PON Port 29	MPL2_SFP23_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off
0	PON Port 28	MPL2_SFP22_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off

3.20. Offset 0x20 SFP_TX_Disable_1 Mask (Read& Write)

(TBD)

Bit	Front port	Name	R/W	Reset Value	Description
7	PON Port 22	MASK*MPL2_SFP29_TX_DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.
6	PON Port 23	MASK*MPL2_SFP28_TX_DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.
5	PON Port 26	MASK*MPL2_SFP27_TX_DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.

4	PON Port 27	MASK*MPL2_SFP26_TX _DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.
3	PON Port 30	MASK*MPL2_SFP25_TX _DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.
2	PON Port 31	MASK*MPL2_SFP24_TX _DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.
1	PON Port 29	MASK*MPL2_SFP23_TX _DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.
0	PON Port 28	MASK*MPL2_SFP22_TX _DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.

3.21. Offset 0x21 SFP_TX_Disable_2 (Read& Write)

Bit	Front port	Net Name	R/W	Reset Value	Description
7	PON Port 41	MPL3_SFP37_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off
6	PON Port 40	MPL3_SFP36_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off
5	PON Port 37	MPL3_SFP35_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off
4	PON Port 36	MPL3_SFP34_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off
3	PON Port 33	MPL3_SFP33_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off
2	PON Port 32	MPL3_SFP32_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off
1	PON Port 18	MPL2_SFP31_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off
0	PON Port 19	MPL2_SFP30_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off

3.22. Offset 0x22 SFP_TX_Disable_2 Mask (Read& Write)

(TBD)

Bit	Front port	Name	R/W	Reset Value	Description
7	PON Port 41	MASK*MPL3_SFP37_TX_DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.
6	PON Port 40	MASK*MPL3_SFP36_TX_DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.
5	PON Port 37	MASK*MPL3_SFP35_TX_DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.
4	PON Port 36	MASK*MPL3_SFP34_TX_DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.
3	PON Port 33	MASK*MPL3_SFP33_TX_DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.
2	PON Port 32	MASK*MPL3_SFP32_TX_DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.
1	PON Port 18	MASK*MPL2_SFP31_TX_DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.
0	PON Port 19	MASK*MPL2_SFP30_TX_DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.

3.23. Offset 0x23 SFP_TX_Disable_3 (Read& Write)

Bit	Front port	Net Name	R/W	Reset Value	Description
7:5		Reserved			
4	PON Port 43	MPL3_SFP42_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off
3	PON Port 46	MPL3_SFP41_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off
2	PON Port 47	MPL3_SFP40_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off
1	PON	MPL3_SFP39_TX_DIS	R/W	1	0: Transmitter output is turned on

	Port 45				1: Transmitter output is turned off
0	PON Port 44	MPL3_SFP38_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off

3.24. Offset 0x24 SFP_TX_Disable_3 Mask (Read& Write)

(TBD)

Bit	Front port	Name	R/W	Reset Value	Description
7:5		Reserved			
4	PON Port 43	MASK*MPL3_SFP42_TX_DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.
3	PON Port 46	MASK*MPL3_SFP41_TX_DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.
2	PON Port 47	MASK*MPL3_SFP40_TX_DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.
1	PON Port 45	MASK*MPL3_SFP39_TX_DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.
0	PON Port 44	MASK*MPL3_SFP38_TX_DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.

3.25. Offset 0x25 SFP28_TX_Disable (Read& Write)

Bit	Front port	Net Name	R/W	Reset Value	Description
7	25G Port 7	SFP28_P7_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off
6	25G Port 6	SFP28_P6_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off
5	25G Port 5	SFP28_P5_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off
4	25G	SFP28_P4_TX_DIS	R/W	1	0: Transmitter output is turned on

	Port 4				1: Transmitter output is turned off
3	25G Port 3	SFP28_P3_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off
2	25G Port 2	SFP28_P2_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off
1	25G Port 1	SFP28_P1_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off
0	25G Port 0	SFP28_P0_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off

3.26. Offset 0x26 SFP28_TX_Disable Mask (Read& Write)

(TBD)

Bit	Front port	Name	R/W	Reset Value	Description
7	25G Port 7	MASK*SFP28_P7_TX_DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.
6	25G Port 6	MASK*SFP28_P6_TX_DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.
5	25G Port 5	MASK*SFP28_P5_TX_DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.
4	25G Port 4	MASK*SFP28_P4_TX_DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.
3	25G Port 3	MASK*SFP28_P3_TX_DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.
2	25G Port 2	MASK*SFP28_P2_TX_DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.
1	25G Port 1	MASK*SFP28_P1_TX_DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.
0	25G Port 0	MASK*SFP28_P0_TX_DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.

3.27. Offset 0x27 SFP_LED_ACT (Read& Write)

Bit	Front port	Name	R/W	Reset Value	Description
7	PON Port 22	SFP29_LED_ACT	R/W	1	Steady: No traffic Blinking: Indicates data traffic on the PON
6	PON Port 23	SFP28_LED_ACT	R/W	1	Steady: No traffic Blinking: Indicates data traffic on the PON
5	PON Port 26	SFP27_LED_ACT	R/W	1	Steady: No traffic Blinking: Indicates data traffic on the PON
4	PON Port 27	SFP26_LED_ACT	R/W	1	Steady: No traffic Blinking: Indicates data traffic on the PON
3	PON Port 30	SFP25_LED_ACT	R/W	1	Steady: No traffic Blinking: Indicates data traffic on the PON
2	PON Port 31	SFP24_LED_ACT	R/W	1	Steady: No traffic Blinking: Indicates data traffic on the PON
1	PON Port 29	SFP23_LED_ACT	R/W	1	Steady: No traffic Blinking: Indicates data traffic on the PON
0	PON Port 28	SFP22_LED_ACT	R/W	1	Steady: No traffic Blinking: Indicates data traffic on the PON

3.28. Offset 0x28 SFP_LED_ACT (Read& Write)

Bit	Front port	Name	R/W	Reset Value	Description
7	PON Port 41	SFP37_LED_ACT	R/W	1	Steady: No traffic Blinking: Indicates data traffic on the PON
6	PON Port 40	SFP36_LED_ACT	R/W	1	Steady: No traffic Blinking: Indicates data traffic on the PON
5	PON Port 37	SFP35_LED_ACT	R/W	1	Steady: No traffic Blinking: Indicates data traffic on the PON
4	PON Port 36	SFP34_LED_ACT	R/W	1	Steady: No traffic Blinking: Indicates data traffic on the PON

3	PON Port 33	SFP33_LED_ACT	R/W	1	Steady: No traffic Blinking: Indicates data traffic on the PON
2	PON Port 32	SFP32_LED_ACT	R/W	1	Steady: No traffic Blinking: Indicates data traffic on the PON
1	PON Port 18	SFP31_LED_ACT	R/W	1	Steady: No traffic Blinking: Indicates data traffic on the PON
0	PON Port 19	SFP30_LED_ACT	R/W	1	Steady: No traffic Blinking: Indicates data traffic on the PON

3.29. Offset 0x29 SFP_LED_ACT (Read& Write)

Bit	Front port	Name	R/W	Reset Value	Description
7:5		Reserved			
4	PON Port 43	SFP42_LED_ACT	R/W	1	Steady: No traffic Blinking: Indicates data traffic on the PON
3	PON Port 46	SFP41_LED_ACT	R/W	1	Steady: No traffic Blinking: Indicates data traffic on the PON
2	PON Port 47	SFP40_LED_ACT	R/W	1	Steady: No traffic Blinking: Indicates data traffic on the PON
1	PON Port 45	SFP39_LED_ACT	R/W	1	Steady: No traffic Blinking: Indicates data traffic on the PON
0	PON Port 44	SFP38_LED_ACT	R/W	1	Steady: No traffic Blinking: Indicates data traffic on the PON

3.30. Offset 0x30 SFP_LED_LINK_G (Read& Write)

Bit	Front port	Name	R/W	Reset Value	Description
7	PON Port 22	SFP29_LED_LINK_G	R/W	1	0: PON link up & 1 or more ONTs in service 1: No ONT in service
6	PON Port 23	SFP28_LED_LINK_G	R/W	1	0: PON link up & 1 or more ONTs in service 1: No ONT in service

5	PON Port 26	SFP27_LED_LINK _G	R/W	1	0: PON link up & 1 or more ONTs in service 1: No ONT in service
4	PON Port 27	SFP26_LED_LINK _G	R/W	1	0: PON link up & 1 or more ONTs in service 1: No ONT in service
3	PON Port 30	SFP25_LED_LINK _G	R/W	1	0: PON link up & 1 or more ONTs in service 1: No ONT in service
2	PON Port 31	SFP24_LED_LINK _G	R/W	1	0: PON link up & 1 or more ONTs in service 1: No ONT in service
1	PON Port 29	SFP23_LED_LINK _G	R/W	1	0: PON link up & 1 or more ONTs in service 1: No ONT in service
0	PON Port 28	SFP22_LED_LINK _G	R/W	1	0: PON link up & 1 or more ONTs in service 1: No ONT in service

3.31. Offset 0x31 SFP_LED_LINK_G (Read& Write)

Bit	Front port	Name	R/W	Reset Value	Description
7	PON Port 41	SFP37_LED_LINK _G	R/W	1	0: PON link up & 1 or more ONTs in service 1: No ONT in service
6	PON Port 40	SFP36_LED_LINK _G	R/W	1	0: PON link up & 1 or more ONTs in service 1: No ONT in service
5	PON Port 37	SFP35_LED_LINK _G	R/W	1	0: PON link up & 1 or more ONTs in service 1: No ONT in service
4	PON Port 36	SFP34_LED_LINK _G	R/W	1	0: PON link up & 1 or more ONTs in service 1: No ONT in service
3	PON Port 33	SFP33_LED_LINK _G	R/W	1	0: PON link up & 1 or more ONTs in service 1: No ONT in service
2	PON Port 32	SFP32_LED_LINK _G	R/W	1	0: PON link up & 1 or more ONTs in service 1: No ONT in service
1	PON Port 18	SFP31_LED_LINK _G	R/W	1	0: PON link up & 1 or more ONTs in service 1: No ONT in service
0	PON Port 19	SFP30_LED_LINK _G	R/W	1	0: PON link up & 1 or more ONTs in service 1: No ONT in service

3.32. Offset 0x32 SFP_LED_LINK_G (Read& Write)

Bit	Front port	Name	R/W	Reset Value	Description
7:5		Reserved			
4	PON Port 43	SFP42_LED_LINK _G	R/W	1	0: PON link up & 1 or more ONTs in service 1: No ONT in service
3	PON Port 46	SFP41_LED_LINK _G	R/W	1	0: PON link up & 1 or more ONTs in service 1: No ONT in service
2	PON Port 47	SFP40_LED_LINK _G	R/W	1	0: PON link up & 1 or more ONTs in service 1: No ONT in service
1	PON Port 45	SFP39_LED_LINK _G	R/W	1	0: PON link up & 1 or more ONTs in service 1: No ONT in service
0	PON Port 44	SFP38_LED_LINK _G	R/W	1	0: PON link up & 1 or more ONTs in service 1: No ONT in service

3.33. Offset 0x33 SFP_LED_LINK_B (Read& Write)

Bit	Front port	Name	R/W	Reset Value	Description
7	PON Port 22	SFP29_LED_LINK _B	W	1	0: Port disabled 1: Port enabled
6	PON Port 23	SFP28_LED_LINK _B	W	1	0: Port disabled 1: Port enabled
5	PON Port 26	SFP27_LED_LINK _B	W	1	0: Port disabled 1: Port enabled
4	PON Port 27	SFP26_LED_LINK _B	W	1	0: Port disabled 1: Port enabled
3	PON Port 30	SFP25_LED_LINK _B	W	1	0: Port disabled 1: Port enabled
2	PON Port 31	SFP24_LED_LINK _B	W	1	0: Port disabled 1: Port enabled
1	PON	SFP23_LED_LINK	W	1	0: Port disabled

	Port 29	_B			1: Port enabled
0	PON Port 28	SFP22_LED_LINK _B	W	1	0: Port disabled 1: Port enabled

3.34. Offset 0x34 SFP_LED_LINK_B (Read& Write)

Bit	Front port	Name	R/W	Reset Value	Description
7	PON Port 41	SFP37_LED_LINK _B	W	1	0: Port disabled 1: Port enabled
6	PON Port 40	SFP36_LED_LINK _B	W	1	0: Port disabled 1: Port enabled
5	PON Port 37	SFP35_LED_LINK _B	W	1	0: Port disabled 1: Port enabled
4	PON Port 36	SFP34_LED_LINK _B	W	1	0: Port disabled 1: Port enabled
3	PON Port 33	SFP33_LED_LINK _B	W	1	0: Port disabled 1: Port enabled
2	PON Port 32	SFP32_LED_LINK _B	W	1	0: Port disabled 1: Port enabled
1	PON Port 18	SFP31_LED_LINK _B	W	1	0: Port disabled 1: Port enabled
0	PON Port 19	SFP30_LED_LINK _B	W	1	0: Port disabled 1: Port enabled

3.35. Offset 0x35 SFP_LED_LINK_B (Read& Write)

Bit	Front port	Name	R/W	Reset Value	Description
7:5		Reserved			
4	PON Port 43	SFP42_LED_LINK _B	W	1	0: Port disabled 1: Port enabled
3	PON Port 46	SFP41_LED_LINK _B	W	1	0: Port disabled 1: Port enabled

2	PON Port 47	SFP40_LED_LINK _B	W	1	0: Port disabled 1: Port enabled
1	PON Port 45	SFP39_LED_LINK _B	W	1	0: Port disabled 1: Port enabled
0	PON Port 44	SFP38_LED_LINK _B	W	1	0: Port disabled 1: Port enabled

3.36. Offset 0x36 SFP_LED_LINK_R (Read& Write)

Bit	Front port	Name	R/W	Reset Value	Description
7	PON Port 22	SFP29_LED_LINK _R	W	1	0: Fault detected 1: Normal operation
6	PON Port 23	SFP28_LED_LINK _R	W	1	0: Fault detected 1: Normal operation
5	PON Port 26	SFP27_LED_LINK _R	W	1	0: Fault detected 1: Normal operation
4	PON Port 27	SFP26_LED_LINK _R	W	1	0: Fault detected 1: Normal operation
3	PON Port 30	SFP25_LED_LINK _R	W	1	0: Fault detected 1: Normal operation
2	PON Port 31	SFP24_LED_LINK _R	W	1	0: Fault detected 1: Normal operation
1	PON Port 29	SFP23_LED_LINK _R	W	1	0: Fault detected 1: Normal operation
0	PON Port 28	SFP22_LED_LINK _R	W	1	0: Fault detected 1: Normal operation

3.37. Offset 0x37 SFP_LED_LINK_R (Read& Write)

Bit	Front port	Name	R/W	Reset Value	Description
7	PON Port 41	SFP37_LED_LINK _R	W	1	0: Fault detected 1: Normal operation
6	PON	SFP36_LED_LINK	W	1	0: Fault detected

	Port 40	_R			1: Normal operation
5	PON Port 37	SFP35_LED_LINK _R	W	1	0: Fault detected 1: Normal operation
4	PON Port 36	SFP34_LED_LINK _R	W	1	0: Fault detected 1: Normal operation
3	PON Port 33	SFP33_LED_LINK _R	W	1	0: Fault detected 1: Normal operation
2	PON Port 32	SFP32_LED_LINK _R	W	1	0: Fault detected 1: Normal operation
1	PON Port 18	SFP31_LED_LINK _R	W	1	0: Fault detected 1: Normal operation
0	PON Port 19	SFP30_LED_LINK _R	W	1	0: Fault detected 1: Normal operation

3.38. Offset 0x38 SFP_LED_LINK_R (Read& Write)

Bit	Front port	Name	R/W	Reset Value	Description
7:5		Reserved			
4	PON Port 43	SFP42_LED_LINK _R	W	1	0: Fault detected 1: Normal operation
3	PON Port 46	SFP41_LED_LINK _R	W	1	0: Fault detected 1: Normal operation
2	PON Port 47	SFP40_LED_LINK _R	W	1	0: Fault detected 1: Normal operation
1	PON Port 45	SFP39_LED_LINK _R	W	1	0: Fault detected 1: Normal operation
0	PON Port 44	SFP38_LED_LINK _R	W	1	0: Fault detected 1: Normal operation

3.39. Offset 0x39 SFP28_LED_LINK_G (Read& Write)

Bit	Front port	Name	R/W	Reset Value	Description
7	25G Port 7	SFP28_P7_LED_LINK_G	W	1	0: Link up (speed 25G) 1: Link down Blinking: Indicates data traffic on the PON
6	25G Port 6	SFP28_P6_LED_LINK_G	W	1	0: Link up (speed 25G) 1: Link down Blinking: Indicates data traffic on the PON
5	25G Port 5	SFP28_P5_LED_LINK_G	W	1	0: Link up (speed 25G) 1: Link down Blinking: Indicates data traffic on the PON
4	25G Port 4	SFP28_P4_LED_LINK_G	W	1	0: Link up (speed 25G) 1: Link down Blinking: Indicates data traffic on the PON
3	25G Port 3	SFP28_P3_LED_LINK_G	W	1	0: Link up (speed 25G) 1: Link down Blinking: Indicates data traffic on the PON
2	25G Port 2	SFP28_P2_LED_LINK_G	W	1	0: Link up (speed 25G) 1: Link down Blinking: Indicates data traffic on the PON
1	25G Port 1	SFP28_P1_LED_LINK_G	W	1	0: Link up (speed 25G) 1: Link down Blinking: Indicates data traffic on the PON
0	25G Port 0	SFP28_P0_LED_LINK_G	W	1	0: Link up (speed 25G) 1: Link down Blinking: Indicates data traffic on the PON

3.40. Offset 0x40 SFP28_LED_LINK_B (Read& Write)

Bit	Front port	Name	R/W	Reset Value	Description
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7	25G Port 7	SFP28_P7_LED_L INK_B	W	1	0: Link up (speed 10G) 1: Link down Blinking: Indicates data traffic on the PON
6	25G Port 6	SFP28_P6_LED_L INK_B	W	1	0: Link up (speed 10G) 1: Link down Blinking: Indicates data traffic on the PON
5	25G Port 5	SFP28_P5_LED_L INK_B	W	1	0: Link up (speed 10G) 1: Link down Blinking: Indicates data traffic on the PON
4	25G Port 4	SFP28_P4_LED_L INK_B	W	1	0: Link up (speed 10G) 1: Link down Blinking: Indicates data traffic on the PON
3	25G Port 3	SFP28_P3_LED_L INK_B	W	1	0: Link up (speed 10G) 1: Link down Blinking: Indicates data traffic on the PON
2	25G Port 2	SFP28_P2_LED_L INK_B	W	1	0: Link up (speed 10G) 1: Link down Blinking: Indicates data traffic on the PON
1	25G Port 1	SFP28_P1_LED_L INK_B	W	1	0: Link up (speed 10G) 1: Link down Blinking: Indicates data traffic on the PON
0	25G Port 0	SFP28_P0_LED_L INK_B	W	1	0: Link up (speed 10G) 1: Link down Blinking: Indicates data traffic on the PON

3.41. Offset 0x41 SFP28_LED_LINK_O (Read& Write)

Bit	Front port	Name	R/W	Reset Value	Description
7	25G Port 7	SFP28_P7_LED_L INK_O	W	1	0: Link up (speed 1G) 1: Link down Blinking: Indicates data traffic on the PON

6	25G Port 6	SFP28_P6_LED_L INK_O	W	1	0: Link up (speed 1G) 1: Link down Blinking: Indicates data traffic on the PON
5	25G Port 5	SFP28_P5_LED_L INK_O	W	1	0: Link up (speed 1G) 1: Link down Blinking: Indicates data traffic on the PON
4	25G Port 4	SFP28_P4_LED_L INK_O	W	1	0: Link up (speed 1G) 1: Link down Blinking: Indicates data traffic on the PON
3	25G Port 3	SFP28_P3_LED_L INK_O	W	1	0: Link up (speed 1G) 1: Link down Blinking: Indicates data traffic on the PON
2	25G Port 2	SFP28_P2_LED_L INK_O	W	1	0: Link up (speed 1G) 1: Link down Blinking: Indicates data traffic on the PON
1	25G Port 1	SFP28_P1_LED_L INK_O	W	1	0: Link up (speed 1G) 1: Link down Blinking: Indicates data traffic on the PON
0	25G Port 0	SFP28_P0_LED_L INK_O	W	1	0: Link up (speed 1G) 1: Link down Blinking: Indicates data traffic on the PON

3.42. Offset 0x42 SFP28_RS0 (Read& Write)

Bit	Front port	Name	R/W	Reset Value	Description
7	25G Port 7	SFP28_P7_TRX_R ST	W	1	Rx Rate Select: Open or Low =10.3 Gb/s or 9.8Gb/s High =25.78 Gb/s or 24.33Gb/s
6	25G Port 6	SFP28_P6_TRX_R ST	W	1	Rx Rate Select: Open or Low =10.3 Gb/s or 9.8Gb/s High =25.78 Gb/s or 24.33Gb/s
5	25G Port 5	SFP28_P5_TRX_R ST	W	1	Rx Rate Select: Open or Low =10.3 Gb/s or 9.8Gb/s

					High =25.78 Gb/s or 24.33Gb/s
4	25G Port 4	SFP28_P4_TRX_R ST	W	1	Rx Rate Select: Open or Low =10.3 Gb/s or 9.8Gb/s High =25.78 Gb/s or 24.33Gb/s
3	25G Port 3	SFP28_P3_TRX_R ST	W	1	Rx Rate Select: Open or Low =10.3 Gb/s or 9.8Gb/s High =25.78 Gb/s or 24.33Gb/s
2	25G Port 2	SFP28_P2_TRX_R ST	W	1	Rx Rate Select: Open or Low =10.3 Gb/s or 9.8Gb/s High =25.78 Gb/s or 24.33Gb/s
1	25G Port 1	SFP28_P1_TRX_R ST	W	1	Rx Rate Select: Open or Low =10.3 Gb/s or 9.8Gb/s High =25.78 Gb/s or 24.33Gb/s
0	25G Port 0	SFP28_P0_TRX_R ST	W	1	Rx Rate Select: Open or Low =10.3 Gb/s or 9.8Gb/s High =25.78 Gb/s or 24.33Gb/s

3.43. Offset 0x43 SFP28_RS1 (Read& Write)

Bit	Front port	Name	R/W	Reset Value	Description
7	25G Port 7	SFP28_P7_RSSI	W	1	Tx Rate Select: Open or Low =10.3 Gb/s or 9.8Gb/s High =25.78 Gb/s or 24.33Gb/s
6	25G Port 6	SFP28_P6_RSSI	W	1	Tx Rate Select: Open or Low =10.3 Gb/s or 9.8Gb/s High =25.78 Gb/s or 24.33Gb/s
5	25G Port 5	SFP28_P5_RSSI	W	1	Tx Rate Select: Open or Low =10.3 Gb/s or 9.8Gb/s High =25.78 Gb/s or 24.33Gb/s
4	25G Port 4	SFP28_P4_RSSI	W	1	Tx Rate Select: Open or Low =10.3 Gb/s or 9.8Gb/s High =25.78 Gb/s or 24.33Gb/s
3	25G	SFP28_P3_RSSI	W	1	Tx Rate Select:

	Port 3				Open or Low =10.3 Gb/s or 9.8Gb/s High =25.78 Gb/s or 24.33Gb/s
2	25G Port 2	SFP28_P2_RSSI	W	1	Tx Rate Select: Open or Low =10.3 Gb/s or 9.8Gb/s High =25.78 Gb/s or 24.33Gb/s
1	25G Port 1	SFP28_P1_RSSI	W	1	Tx Rate Select: Open or Low =10.3 Gb/s or 9.8Gb/s High =25.78 Gb/s or 24.33Gb/s
0	25G Port 0	SFP28_P0_RSSI	W	1	Tx Rate Select: Open or Low =10.3 Gb/s or 9.8Gb/s High =25.78 Gb/s or 24.33Gb/s

3.44. Offset 0x44 SFP28_RX_LOS (Read& Write)

Bit	Front port	Name	R/W	Reset Value	Description
7	25G Port 7	SFP28_P7_ED	R	1	0: Normal operation 1: Loss of signal indication
6	25G Port 6	SFP28_P6_ED	R	1	0: Normal operation 1: Loss of signal indication
5	25G Port 5	SFP28_P5_ED	R	1	0: Normal operation 1: Loss of signal indication
4	25G Port 4	SFP28_P4_ED	R	1	0: Normal operation 1: Loss of signal indication
3	25G Port 3	SFP28_P3_ED	R	1	0: Normal operation 1: Loss of signal indication
2	25G Port 2	SFP28_P2_ED	R	1	0: Normal operation 1: Loss of signal indication
1	25G Port 1	SFP28_P1_ED	R	1	0: Normal operation 1: Loss of signal indication
0	25G Port 0	SFP28_P0_ED	R	1	0: Normal operation 1: Loss of signal indication

3.45. Offset 0x45 Reserve_1 (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:6	Reserved			
5	CPLD3_CPLD2_RESERVE_C	R/W	1	Reserve from CPLD3 to CPLD2
4	CPLD3_CPLD2_RESERVE_B	R/W	1	Reserve from CPLD3 to CPLD2
3	CPLD3_CPLD2_RESERVE_A	R/W	1	Reserve from CPLD3 to CPLD2
2	CPLD2_CPLD1_RESERVE_C	R/W	1	Reserve from CPLD2 to CPLD1
1	CPLD2_CPLD1_RESERVE_B	R/W	1	Reserve from CPLD2 to CPLD1
0	CPLD2_CPLD1_RESERVE_A	R/W	1	Reserve from CPLD2 to CPLD1

3.46. Offset 0x46 Reserve_2 (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:3	Reserved			
2	FPGA1_CPLD2_RESERVE_E	R/W	1	Reserve from FPGA1 to CPLD2
1	FPGA1_CPLD2_RESERVE_D	R/W	1	Reserve from FPGA1 to CPLD2
0	FPGA1_CPLD2_RESERVE_B	R/W	1	Reserve from FPGA1 to CPLD2

3.47. Offset 0x47 Maple debug console (Read& Write)

Front port	Name	S2	S1	S0
Port 0 to Port 15	Maple 1console	0	0	0
Port 16 to Port 31	Maple 2 console	0	0	1
Port 32 to Port 47	Maple 3 console	0	1	0
Port 48 to Port 63	Maple 4 console	0	1	1

Maple console control table

Control the register to change the maple debug console.

Bit	Name	R/W	Reset Value	Description
7:3	Reserved			
2	MAPPLE_MUX_S2	R/W	0	Detail refer to above maple console control table.
1	MAPPLE_MUX_S1	R/W	0	Detail refer to above maple console control table.
0	MAPPLE_MUX_S0	R/W	0	Detail refer to above maple console control table.

3.48. Offset 0x48 MGMT SFP (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:6	Reserved	R	0	
5	Reserved	R	0	
4	MGMT_SFP_TRX_RST	R	0	Reserve
3	MGMT_SFP_ED	R/W	0	0: Normal operation 1: Loss of signal indication
2	MGMT_SFP_TX_DIS	R/W	0	0: Transmitter output is turned on 1: Transmitter output is turned off
1	MGMT_SFP_TX_FAULT	R/W	0	1: MGMT SFP Transmit Fault 0: MGMT SFP Transmitter is working well
0	MGMT_SFP_MOD_ABS	R/W	1	0: MGMT SFP transceiver is present 1: MGMT SFP transceiver is absent

3.49. Offset 0x49 CPU I2C (Read& Write)

(TBD)

Bit	Name	R/W	Reset Value	Description
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7:4	Reserved			
1	CPLD_2_CPU_SDA	R/W		SDA from CPU to CPLD2
0	CPLD_2_CPU_SCL	R/W		SCL from CPU to CPLD2

3.50. Offset 0x4A LED Stream (Read& Write)

(TBD)

Bit	Name	R/W	Reset Value	Description
7:4	Reserved			
3	CPLD2_PON_LED_DATA	R/W		PON LED DATA from FPGA2 to CPLD2
2	CPLD2_PON_LED_CLK	R/W		PON LED CLK from FPGA2 to CPLD2
1	CPLD2_UPLINK_LED_DATA	R/W		Uplink LED DATA from FPGA2 to CPLD2
0	CPLD2_UPLINK_LED_CLK	R/W		Uplink LED CLK from FPGA2 to CPLD2

4.1. Offset 0x01 Reset Input (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:1	Reserved			
0	CPLD3_TO_CPLD2_RESET	R	1	0: Normal operation 1: Reset CPLD2 by SW

4.2. Offset 0x02 Power Present (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:1	Reserved			
0	MAIN_BOARD_POWER_PRESENT_4	R	0	0: Main board power off 1: Main board power on

4.3. Offset 0x03 MAPLE Reset Output (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:4	Reserved			
3	MPL4_RESET_OUT_L	R	1	0: Reset output from MAPLE4
2	MPL3_RESET_OUT_L	R	1	0: Reset output from MAPLE3
1	MPL2_RESET_OUT_L	R	1	0: Reset output from MAPLE2
0	MPL1_RESET_OUT_L	R	1	0: Reset output from MAPLE1

4.4. Offset 0x04 BMC I2C (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:4	Reserved			
1	CPLD_2_BMC_SDA	R/W		SDA from BMC to CPLD2
0	CPLD_2_BMC_SCL	R/W		SCL from BMC to CPLD2

4.5. Offset 0x05 Interrupt Stream (Read& Write)

(TBD)

Bit	Name	R/W	Reset Value	Description
7:4	Reserved			
1	CPLD2_TO_FPGA2_INTERRUPT_DATA	R/W		Interrupt DATA from CPLD2 to FPGA2
0	CPLD2_TO_FPGA2_INTERRUPT_CLK	R/W		Interrupt CLK from CPLD2 to FPGA2